REMARKS

The above amendments are made in response to the first Office Action mailed June 15, 2005, wherein:

1. Claim 3 was objected to as having an informality;
2. Claims 1-4 and 15 were rejected under 35 U.S.C. § 102(a) as being anticipated by published U.S. Patent No. 6,847,555 to Toda (the "Toda patent");
3. Claims 12 and 38 were rejected under 35 U.S.C. § 103(a) as being obvious over the Toda patent in view of U.S. Patent Publication No. 2002/0021605 to Harada, et al., (The "Harada application"); and
4. Claims 5-11, 13, 14, 16-20, and 39-40 were indicated as being allowable if rewritten in independent form.

Applicants acknowledge with appreciation the Examiner's notation of the error in Claim 3 and the tentative allowance of Claims 5-11, 13-14, 16-20, and 39-40 if rewritten in independent form. With this Amendment, Claim 1 has been amended to include subject matter from Claims 2, 4, and 15, and Claim 3 has been amended to have strict antecedent basis to the language in Claim 1. Below, Applicants provide the reasons as to why amended Claim 1 is allowable over the Toda patent. Claims 2, 4, and 15 have been canceled without prejudice, and Claims 3 and 5-12 have been amended to correspond to the amendments to Claim 1 and/or to remove duplicative language. Also, rejected independent Claim 38 has been amended to include the subject matter from tentatively allowed Claim 5; reasons are provided below as to why amended Claim 38 is allowable over the prima facie combination of the Toda patent and the Harada application. Additionally, new dependent Claims 41-44 have been added (each being dependent directly or indirectly from independent Claim 38), and new claims 45-60 have been added to effect the rewriting of dependent Claims 5-11, 13-14, and 16-20 in independent form. The support for these new claims is provided below. Finally, withdrawn Claims 21-37 are canceled without prejudice with this amendment in response to the prior restriction requirement. **In summary, Claims 1, 3, 5-14, 16-20, 38-40, and new Claims 41-60 are pending in the application.**

Response to the Rejection of Claims 1 and 3

Claims 1-4 and 15 were rejected as being anticipated by the Toda patent. The rejection was primarily based on the program verification circuitry of the Toda patent. This circuitry is different from Toda's read circuitry, which is used to read the data values of the memory cells. Applicants respectfully submit that amended Claim 1 recites a combination of a memory structure and read circuit which is different from the program verification circuitry and read circuitry of the Toda patent, and which is novel and non-obvious thereover.

The Toda patent discloses in its FIG. 1 a flash memory device having two cell arrays (1t and 1c) disposed on either side of a row of sense amplifiers (3). The cells in the top array (1t) are called "true" cells, and the cells in the bottom array are called "complementary" cells. Each true cell is **paired** with a complementary cell in order to cooperatively store two data bits simultaneously: which Toda calls the "high bit" and the "low bit." Each cell, whether true or complementary, can be programmed with four different states of charge, as indicated in FIG. 3 of the Toda patent, which are designated herein as charge states 1-4, with charge state 1 producing the lowest cell threshold voltage, and charge state 4 producing the highest cell threshold voltage. An annotated copy of Toda's FIG. 3 is attached showing these states. The charge states for a pair of cells are **coordinated** in the following balanced manner: when one of the paired cells is programmed with charge state 1, the other is programmed with charge state 4; and when one of the pair cells is programmed with charge state 2, the other is programmed with charge state 3. This is illustrated by the crossing lines in the middle of Toda's FIG. 3. The two cells store the combination of a "high bit" and a "low bit," which are read out by a multi-step reading process that is described starting at column 5, line 60, of the Toda patent. ***In each of these read steps, both memory cells of the pair are selected at the same time with voltages applied to the word lines that are coupled to the memory cells.*** The levels of the applied voltages are set such that one memory cell of the pair conducts a current while the other cell does not (see Toda patent, column 5, line 60 through to column 6, line 9, read in light of the locations of the read voltages R1-R3 in Toda's FIG. 3 relative to the four charge-state distributions shown in Toda's FIG. 3).

In contrast to the read circuitry of the Toda patent, the last paragraph of amended Claim 1 recites a read circuit that selects only one memory cell from the first plurality or the second

plurality of memory cells[1] ("said read circuit providing an activation signal to the read-select input of only one of the first plurality or second plurality of memory cells at a time"). Accordingly, amended Claim 1 is clearly different from the read circuitry of the Toda patent and is not anticipated by it. Furthermore, since the central inventive feature of the Toda patent is to have two paired cells collectively store a high bit and low bit which are read out when both cells of the pair are selected for reading, it would not be obvious to modify the Toda patent to select only one memory cell of a pair for reading. This is true regardless of the teachings of any other prior art reference, including the Harada application.

In the Toda patent, the charge state for each memory cell of a pair is separately set by a program-verification process. This process is described at column 6 (starting at line 40) through column 9 of his patent, and is illustrated by his FIGS. 5-8. After erasing the memory cell, Toda's process alternates between incremental programming pulses and verification steps until the threshold voltage of the memory cell exceeds that of a verify voltage Vr. During a verification step, the memory cell is coupled to one input of a sense amplifier (31 in FIG. 8), and a reference current source Io (36 in FIG. 8) is coupled to the other input of the sense amplifier through either of transistors MP0 or MP1. When the memory cell is finally programmed to a charge state that represents a desired data state, it **always** conducts substantially less current than that conducted by reference current source Io (see the paragraph at column 8, lines 11-29 of the Toda patent, and in particular lines 20-23 of column 8).[2]

In contrast to the verification step of the Toda patent, a memory cell from the first or second plurality of memory cells generates a current (I_{M1} or I_{M2}) that is greater than the current generated by the reference current circuit (I_{R1} or I_{R2}, respectively) when the memory cell represents one of the data states. Specifically, each memory cell recited by amended Claim 1 generates a non-zero current (I_{M1} or I_{M2}) at its read output to represent one of the data states, and generates a substantially zero current to represent another of the data states (see the first and

[1] In the Office Action, the Rejection indicated that the first plurality of memory cells recited by Claim 1 read on Toda's array of true cells, and that the second plurality of memory cells read on Toda's array of complementary memory cells.

[2] In the Office Action, the Rejection relied upon a statement at column 7, lines 64-67 of the Toda patent. However, this statement applies to an **erased** memory cell that has not yet been fully programmed to properly represent a data state.

second paragraphs of the body of amended Claim 1). As indicated in the fifth and sixth paragraphs of amended Claim 1, the reference currents (I_{R1} and I_{R2}) are less than the larger currents generated by the memory cells (I_{M1} and I_{M2}, respectively). As indicated above, when Toda's memory cell is programmed to the charge state that represents the desired data state, the cell always conducts a current that is substantially less than Toda's reference current source. Accordingly, amended Claim 1 is clearly different from the verification circuitry of the Toda patent and is not anticipated by it. Furthermore, Applicants respectfully submit that it would not be obvious to modify Toda's verification step to do otherwise because of Toda's criterion for determining when his memory cell has been properly programmed. This criterion requires that the sense amplifier place Toda's data latch 32 in a specific state, which in turn requires the current from the programmed memory cell to be less than the reference current (see, for example, Toda patent at column 8, lines 11-34, particularly lines 22-34). This is true regardless of the teachings of any other prior art reference, including the Harada application.

Since amended Claim 1 is not anticipated or obvious over the read circuitry and verification circuitry of the Toda patent, it is respectfully submitted that the Toda patent does not teach or suggest amended Claim 1.

Claim 3 is dependent on amended Claim 1, and is novel and non-obvious over the Toda patent for the same reasons as amended Claim 1.

Response to the Rejection of Claims 12 and 38

Claims 12 and 38 were rejected under 35 U.S.C. § 103(a) as being obvious over the Toda patent in view of the Harada application. Claim 12 is dependent upon amended Claim 1, and is allowable for the same reasons as amended Claim 1. With this Amendment, amended Claim 38 now recites subject matter from Claims 5 and 6. Specifically, amended Claim 1 recites specific relationships between the currents I_{R1} and I_{M1}, and between the currents I_{R2} and I_{M2}. The subject matter of dependent Claims 5 and 6 were indicated as being allowable, and Applicants respectfully submit that amended Claim 38 is allowable for the same reasons as are original dependent Claims 5 and 6.

Furthermore, as to both of Claims 12 and 38, it would not be obvious to modify the Toda patent to follow the current relationship that the Rejection has cited in the Harada application

because such modification would render both the read circuitry and the verification circuitry of the Toda patent inoperative, for the reasons indicated above. Toda's read circuitry does not use a reference at all, and instead uses paired true and complementary memory cells; and Toda's verification circuitry requires that the properly programmed memory cell conduct less current than the reference current in order for his sense amplifier to invert the state of his data latch 32, which terminates the sequence of programming pulses (Toda patent at column 8, lines 11-34, particularly lines 22-34).

Accordingly, it is respectfully submitted that Claims 12 and 38 are non-obvious over the Rejection's *prima facie* combination of the Toda patent and Harada application.

New Claims 41-60

New Claim 41 is dependent upon new Claim 38 and is supported by original Claim 9.

New Claim 42 is dependent upon new Claim 41 and is supported by original Claim 10.

New Claim 43 is dependent upon new Claim 38 and is supported by original Claim 13.

New Claim 44 is dependent upon new Claim 38 and is supported by original Claim 14.

New Claim 45 is original Claim 5 rewritten in independent form.

New Claim 46 is dependent on new Claim 45 and is supported by original Claim 8.

New Claim 47 is dependent on new Claim 45 and is supported by original Claim 9.

New Claim 48 is dependent on new Claim 47 and is supported by original Claim 10.

New Claim 49 is dependent on new Claim 45 and is supported by original Claim 13.

New Claim 50 is dependent on new Claim 45 and is supported by original Claim 16.

New Claim 51 is dependent on new Claim 45 and is supported by original Claim 18.

New Claim 52 is dependent on new Claim 45 and is supported by original Claim 19.

New Claim 53 is original Claim 13 rewritten in independent form.

New Claim 54 is dependent on new Claim 53 and is supported by original Claim 14.

New Claim 55 is dependent on new Claim 53 and is supported by original Claim 16.

New Claim 56 is original Claim 16 rewritten in independent form.

New Claim 57 is dependent upon new Claim 56 and is supported by original Claim 17.

New Claim 58 is original Claim 18 rewritten in independent form.

New Claim 59 is original Claim 19 rewritten in independent form.

New Claim 60 is dependent upon new Claim 59 and is supported by original Claim 20.

CONCLUSION

In view of the remarks made above, Applicants respectfully submit that the application is in condition for allowance and action to that end is respectfully solicited. If the Examiner should feel that a telephone interview would be productive in resolving issues in the case, he is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

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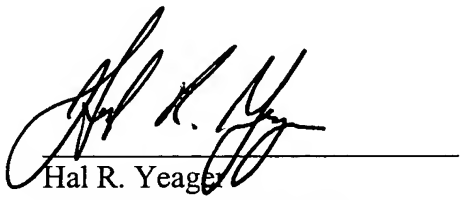
Sheppard Mullin Richter & Hampton LLP
4 Embarcadero Center, 17th Floor
San Francisco, CA 94111-4106
Tel: (415) 434-9100
Fax: (415) 434-3947



Hal R. Yeager
Registration No. 35,419

Annotated FIG 3 of the Toda Patent

FIG. 3